Master's Thesis:

Modelling of Silicon Carbide Power Semiconductor Packages with SiC MOSFETs Based On ANSYS Q3D

Background

Silicon carbide (SiC) is a new power semiconductor material with characteristics which lead to large improvements in energy efficiency when used in the electrical drive system in railway. Both conduction and switching losses can be reduced when SiC is used in the power converter. Greatly reduced switching losses can be achieved compared to the conventional power semiconductor material silicon (Si) used today, if a higher switching speed is used for each switch event. But the faster switching gives rise to higher dv/dt and di/dt which may lead to excessive EMI.

This Master thesis project will be a part of a larger project performed in cooperation between RISE Acreo and Bombardier Transportation. The students will formally belong to RISE Acreo, but it is planned that work will be performed both at RISE Acreo in Kista and at Bombardier Transportation in Västerås.

Objective

The main objective of the present master thesis project is to model the SiC power semiconductors (SiC MOSFETs) when connected in parallel. The approach will be bottom-up, where the semiconductor chip is the starting point and the model is built up to represent multiple semiconductor chips connected in parallel. This type of model can then be used to design the converter, for example by optimizing the gate drive. The students will cooperate with experts modeling 1) the parasitics in the package, using ANSYS Q3D and 2) the semiconductor device chips using TCAD. Using these tools, a detailed 3D model of the power module can be created with chip properties, like device design and doping concentrations, electrical connections, material properties, etc., so that the behavior as shown in the datasheet of the power semiconductor module can be reproduced.

The project will involve the following tasks:

1. Extract package parasitic values from the ANSYS Q3D model of the package, which together with the model of the semiconductor chips, can be used in circuit simulations (for example SPICE, Plecs, Simplorer).
2. Investigate the influence of the parasitic components and develop solutions to overcome potential problems.
3. The ambition is also to verify and characterize the developed model through measurements performed in the lab.

Application

The project can be performed by 1 or 2 students (with adjusted scope).

Prerequisites: Relevant background, *e.g.* Electrical Engineering or Engineering Physics. Knowledge from a course about semiconductor physics is a benefit, as is previous experience of 3D simulation software such as ANSYS or Comsol Multiphysics.

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